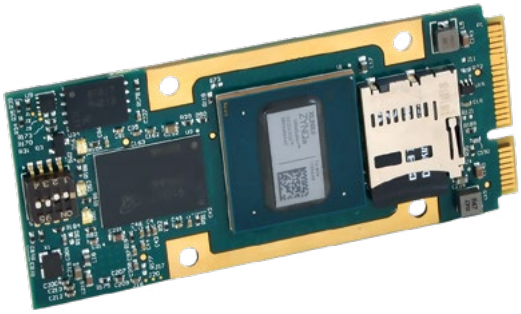
AcroPack® Modules

PRELIMINARY INFORMATION — DATA SUBJECT TO CHANGE

Rugged interconnect™ TECHNOLOGIES
Technologies evolve, our commitment remains

APZU Series User-Configurable Zynq® UltraScale+™ MPSoC I/O Modules

CE · 2 YEAR WARRANTY · RoHS Compliant



APZU-30x with included heat sync attached

Xilinx® Zynq UltraScale+ MPSoC ◆ ARM Cortex™ A53 & R5 CPUs ◆ Programmable logic ◆ PCIe Bus Interface

Models

APZU-301: 28 TTL I/O
APZU-303: 20 TTL and 3 RS485/422
APZU-304: 14 LVDS I/O

Description

The AcroPack product line updates our popular Industry Pack I/O modules with a PCIe interface format. This tech-refresh design offers a compact size with low-cost I/O in a rugged form factor.

The APZU series provides a Xilinx Zynq UltraScale+ multiprocessor system on a chip (MPSoC). This MPSoC integrates a feature-rich ARM-based processing system and programmable logic in a single device. Two dual-core ARM Cortex CPUs (A53 application processor and R5 real-time processor) deliver high-performance computation capability. Additional resources include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. The integrated ASIC-class programmable logic is ideal for compute-intensive tasks and offloading critical applications.

The real value of the Zynq UltraScale+ MPSoC architecture lies in the tight integration of its programmable logic with the processing system. Its high throughput interface eliminates bottlenecks that plague two-chip ASSP-FPGA solutions and allows designers to easily extend the processing system capabilities.

Now designers can build their own custom design by adding peripherals in the programmable logic and increase overall system performance by partitioning HW and SW functions with custom accelerators.

Designed for COTS applications these FPGA based digital I/O modules deliver economical user-customizable I/O in a high-density and very rugged form factor.

AcroPack® modules are 70mm long, only 19mm longer than a full length mini PCIe card and the same 30mm width. They also use the same mPCIe standard connector, board hold down standoff, and screw keep out areas. However, AcroPacks add a down facing 100 pin Samtec connector that mates with the carrier card to eliminate cables and increase reliability. Fifty of these pins are available for field I/O signals.

The Engineering Design Kit provides users with basic information required to develop custom FPGA firmware for download to the Xilinx FPGA. Example FPGA design code is provided as a Vivado® IP Integrator project for functions such as a one-lane PCI Express interface, DMA, digital I/O control register, and more. Users should be fluent in the use of Xilinx Vivado design tools.

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Acromag® THE LEADER IN INDUSTRIAL I/O

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AcroPack® Modules

ISO9001
AS9100
MADE IN USA

Key Features & Benefits

Zynq SoC

- Dual-core ARM Cortex A53-based application processor unit (APU).
- Up to 1.5GHz CPU frequency.
- NEON™ media-processing engine.
- Dual-core ARM Cortex R5-based real-time processor unit (RPU).
- Up to 600MHz CPU frequency.
- Extensive on-chip memory.
- Dedicated I/O peripherals and interfaces.
- Peripherals: USB-UART, I2C.
- Peripherals w/built-in DMA: USB 2.0 high-speed transceiver, 1000BASE-T Ethernet.
- Programmable logic on UltraScale architecture.

XCZU3CG-2SBVA484I

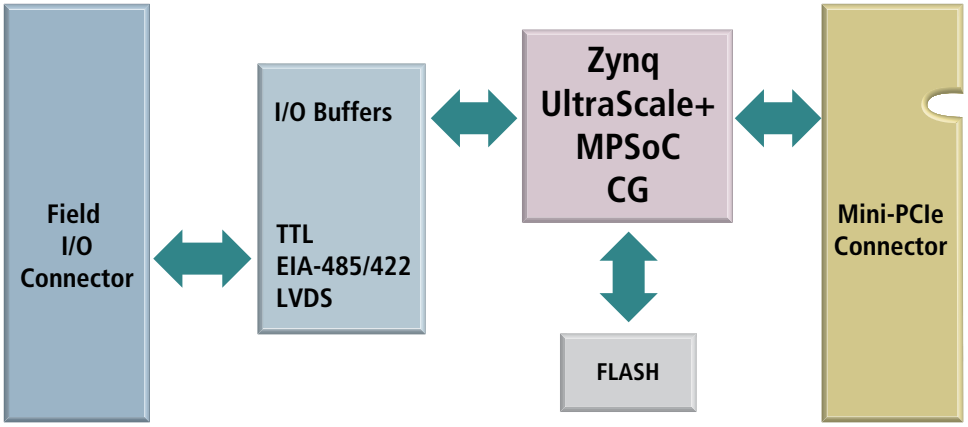
- Up to 154K programmable logic cells.
- Up to 141K flip flops.
- Up to 71K look-up tables (LUTs).
- Up to 7.6Mb block RAM.
- Up to 360 DSP slices.

Digital I/O

- High channel count digital interface: RS485, LVDS and TTL interface options.
- External LVTTL clock input.
- Long distance data transmission.

General

- PCI Express Generation 1 interface.
- 64Mb quad serial flash memory.
- 2 GB (512M x32) LPDDR4 memory.
- DMA transfer support to move data between module memory and PCIe bus.
- Bootable MicroSD Socket.
- Power up and system reset is failsafe.
- Conduction-cooled options.
- Example design.
- USB-UART provides a Zynq debug terminal port.
- Gigabit Ethernet over copper wire 1000BASE-T
- Software development tools for VxWorks®, Linux®, and Windows® environments.



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